Interconnect Stack using Self-Aligned Quad and Double Patterning for 10nm High Volume Manufacturing

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Abstract

This paper describes Intel's 10nm high-performance logic technology interconnect stack featuring 13 metal layers comprising two self-aligned quad patterned and four self-aligned double patterned layers. Quad patterned interconnect layers are introduced to continue Moore's Law, i.e. sub-40nm interconnect pitches to enable 10nm node cells that include 34nm fin pitch and Contact-over-active-gate (COAG) layout. Cobalt metallization is introduced in the pitch quartered interconnect layers in order to meet electromigration and gapfill-resistance requirements.

Introduction

This manuscript is an interconnect-centric overview of Intel's 10nm node process [1], focusing on newer features added since the 14nm process [2, 3] was productized. The 10nm interconnect layer count is unchanged from 14nm at thirteen. However, the lowest five layers extend pitch scaling to sub-50nm dimensions. Three Cu-based 44nm pitches are introduced; these are coupled to the two layers at sub-40nm pitch. The Metal-1 (M1) 36nm minimum pitch represents a 0.51x linear scaling from its mirror layer at the 14nm node, a leap in linear scaling achieved when comparing two successive technology nodes.

A damage-resistant Low K (DR LK) is introduced for the self-aligned pitch quartered (SAQP) and self-aligned pitch doubled (SADP) layers while Low-K carbon doped oxide (LK CDO) is reused for middle pitch layers. The uppermost two metal layers include a dual damascene layer with a thick hard oxide dielectric and an even thicker final metal with a polymer dielectric. Table 1 summarizes the interconnect stack, while Figure 1 depicts the lowest 10 layers.

Table 1: 10nm Interconnect Pitch by Metal Layer

Layer	Patterning	Metal	Dielectric	Pitch (nm)	Scaling vs. 14nm
M0	SAQP	Co	DR LK	40	0.71x
M1	SAQP	Co	DR LK	36	0.51x
M2	SADP	Cu	DR LK	44	0.85x
M3	SADP	Cu	DR LK	44	0.79x
M4	SADP	Cu	DR LK	44	0.55x
M5	SADP	Cu	DR LK	52	0.52x
M6	SAV	Cu	LK CDO	84	0.53x
M7-8	SAV	Cu	LK CDO	112	0.70x
M9-10	SAV	Cu	LK CDO	160	0.63x
Thk M0	Via 1st	Cu	SiO2	1080	1.00x
Thk M1	Plate-up	Cu	Polymer	11000	0.78x

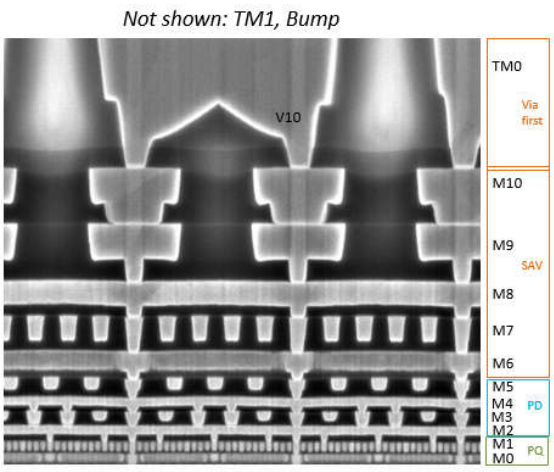

Figure 1: 10nm Interconnect Stack

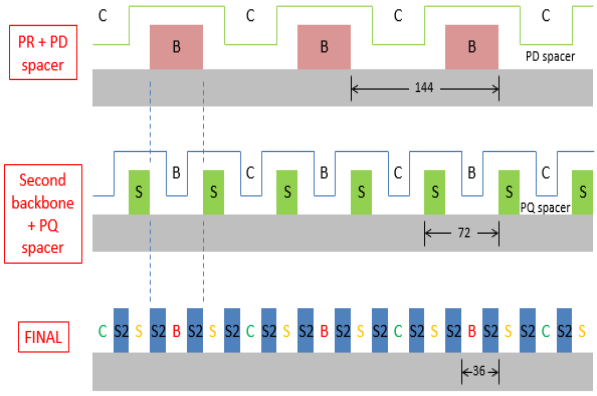

Figure 2: Spacer-based pitch quartering grating principle for 36nm final pitch.

Process Discussion and Results

This interconnect stack forms the basis for Intel's10nm high performance CPU and Low Power products. A self-aligned via (SAV) dual damascene scheme is utilized for M0-M10, except that M0-M1 is pitch quartered and M2-M5 is pitch doubled. In order to realize the technology performance targets, a CDO variant termed DR LK was innovated to preserve capacitance benefits through fine pitch patterning. As in previous generations, each metal layer is resistance targeted to deliver the required current density to meet performance demands without sacrificing reliability.

M0 and M1 are the new quad patterned layers. At 36nm M1 pitch, the lithography requirements are comparatively relaxed, printing at 144nm pitch. Photoresist forms a backbone upon which a pitch doubling spacer is deposited. The pitch doubling spacer in turn becomes the backbone for the pitch quartering spacer. This approach extends grating scaling well below the capabilities of 193nm immersion lithography. The described pitch quartering scheme is illustrated in Figure 2.

With the grating formed, line breaks (or plugs) and vias are patterned using orthogonally oriented layout. The 10nm process uses replacement plugs instead of the traditional masked pattern transfer convention. The replacement method enables via and plug patterning to nominally use the same principles including design rules and litho correction (OPC) that simplifies and synergizes process maintenance. Additionally, replacement plugs permit a choice of dielectric for end-to-end regions. An alumina-based dielectric is used to permit robust insulation while delivering end-to-end critical dimensions below 25nm.

Cobalt metallization is used in M0 and M1. Cobalt's properties provide the required excellent electromigration resistance for high performance designs. At the short range routing distances typical of M0 and M1, the intrinsic resistance penalty of cobalt (vs. copper) is negligible, especially when the true copper volume at sub-40nm pitches is considered. Additionally, mobility of cobalt in low K dielectric is low that permits

a simple titanium-based liner, thereby minimizing interlayer via resistance at these high via count layers. Figure 3 is a top-down image of M0 with the replacement plugs and cobalt metallization and Figure 4 shows the improved via resistance resulting from the Ti-based liner.

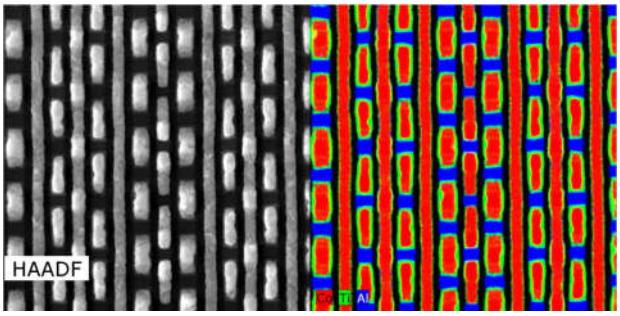

Figure 3: 40nm pitch quartered layer with replacement aluminum oxide plugs and cobalt fill.

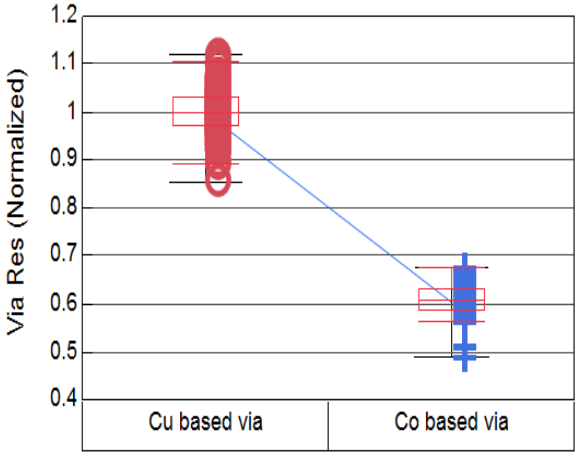

Figure 4: Normalized via resistance comparing cobalt via with Ti-based liner to copper via with Ta-based barrier.

M2-M5 are Intel's second generation SADP layers that extend the minimum pitch to 44nm. The pitch doubling process principles remain unchanged from the 14nm node. Aspect ratios have been maintained in the 1.8-2.2 range for sub-60nm pitch layers to maximize yield. For metallization, the Ta-based barrier is modestly scaled to maintain a high-yielding gapfill process while providing its Cu barrier function. Both cobalt cap and doped copper gapfill options have been used in the 10nm node depending on the current density needs. Figure 5 shows the electromigration benefits of the metallization schemes described.

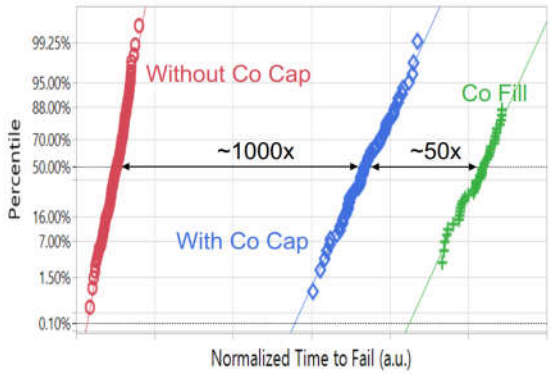

Figure 5: Electromigration results from three interconnect metallization schemes – copper, cobalt-capped copper, and cobalt.

The damage resistant low K CDO film and patterning process delivers ~5% improved capacitance at matched resistance. Figure 6 is an RC comparison between 52nm pitch doubled layers from Intel's 10nm and 14nm nodes illustrating the benefit.

M6-M10 layers at pitches >80nm employ the traditional self-aligned via, dual damascene process with hard mask grating patterning. Metallization is conventional Ta-based barrier with doped Cu electroplated fill.

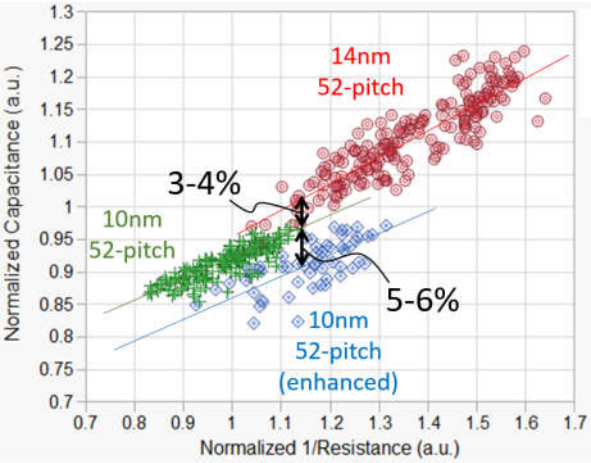

Figure 6: RC comparison showing capacitance benefit with damage resistant low K CDO.

Summary

A high-performance, dense interconnect stack featuring 13 metal layers, including two self-aligned pitch quartering and four self-aligned pitch doubling layers is outlined. This stack delivers the demanding high performance computing needs while meeting all reliability requirements. Microprocessors built on this technology are currently in high volume production at multiple Intel manufacturing facilities.

Acknowledgments

The authors would like to thank their colleagues in Logic Technology Development and Corporate Quality Network, groups for their contributions towards this interconnect technology.

References

[1] C. Auth, et al. "10nm High Performance and Low-Power CMOS Technology Featuring 3rd Generation FinFET Transistors, Self-Aligned Quad Patterning, Contact over Active Gate and Cobalt Local Interconnects," IEDM, 2017.

[2] K. Fischer, et al. "Performance Enhancement for 14nm High Volume Manufacturing Microprocessor and System on a Chip Processes," IITC, 2016.

[3] K. Fischer, et al. "Low-k Interconnect Stack with multi-layer Air Gap and Tri-Metal-Insulator-Metal Capacitors for 14nm High Volume Manufacturing," IITC, 2015.